## REMARKS

This amendment is submitted in response to the Examiner's Action dated March 18, 2004. Applicants have amended the claims to clarify key features of the invention and overcome the claim rejections. Several claims have been added to complete the final two of the claim sets. No new matter has been added, and the features added are fully supported within the specification. The amendments overcome the claim rejections and place the claims in condition for allowance. Applicants respectfully request entry of the amendments to the claims. The discussion/arguments provided below in response to the claim rejections reference the claims in their amended form.

### IN THE SPECIFICATION/ABSTRACT

In the present Office Action, Examiner states that the title is not descriptive. Accordingly, Applicants have provided a new title, which is descriptive of the functional features of the claimed invention. Applicants have also deleted the title from the abstract and amended the specification to correct grammatical or typographical mistakes. Applicants respectfully request entry of the amendments to the specification and removal of the objection to the title.

### CLAIMS REJECTIONS UNDER 35 U.S.C. § 102

In the present Office Action, Claim 12 is rejected under 35 U.S.C. § 102(e) as being anticipated by *McCrory, et al.* (U.S. Patent No. 6,513,057). *McCrory* does not anticipate Applicants' claimed invention because *McCrory* does not teach each feature recited by Applicants' claims.

Applicants' claim now recites additional features not previously recited by the claims. These features are:

"an enhanced operating system (OS) that supports inter-processing operations between said plurality of processors including cache coherency operations based on a collective memory configuration of the processing system, wherein said OS logs operating characteristics and cache topology data of each processor connected to the interconnection means to enable calculation of efficient work allocation among processors;

wherein said system bus and said enhanced operating system support backward and forward compatibility amongst said first processor and said second, heterogenous processor and provides system centric enhancements for inter-processor operations including cache intervention, prefetching, and intelligent cache states"

The above new OS feature and associated functionality is not taught nor suggested by *McCrory*. Notably also, *McCrory* does not teach interrupt pins being used to provide connection for at least one of the processors.

The standard for a § 102 rejection requires that the reference teach each element recited in the claims set forth within the invention. With the above added features to the claims, *McCrory* fails to meet this standard and therefore does not anticipate Applicants' invention.

**CLAIM REJECTIONS UNDER 35 U.S.C. § 103**

In the present Office Action, Claims 1-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over *McCrory* in view of *Jayakumar* (U.S. Patent No. 5,904,733). Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over *McCrory*.

First, there is no motivation in either reference (and none can be found in the art as it existed at the time of Applicants invention) for combining the above references. In fact, absent the teachings of Applicants' claimed invention, the combination would probably not have been made by Examiner.

*McCrory* teaches a heterogenous SMP where the "processors from distinct families ...integrated on a single platform" and "coupled with an implementation specific communication mechanism through family specific bus interface converters" (Abstract). Notably, *McCrory* never actually teaches any interconnect that supports later addition of heterogenous processors, and the processors in *McCorry's* system are specifically described as "integrated" or "packaged". Neither of these two terms connotes the functionality of being able to later add a heterogenous processor via an interconnect means that is designed specifically for that functionality.

*Jayakumar*, which is primarily focused on "selecting a bootstrap processor from among the processors of a multiprocessor system," does mention (in the background) that "additional processors may be added to the SMP without alerting the software." It is, however, very clear to one skilled in the art at the time of Applicants' invention that *Jayakumar* was specifically discussing homogenous systems. In fact, Examiner admits that *Jayakumar* teaches "a traditional SMP environment, while *McCrory* has taught a heterogenous SMP system."

As acknowledged within the Application's background section, addition of homogenous processors to an SMP was known in the art. However, what was not known, and what is in fact the focus of Applicants' invention was how to extend this functionality (i.e., later addition of homogenous processors) to the heterogenous processor environment. Data processing systems were not previously designed with such capability for heterogenous upgrades, particular with processor running at different frequencies and having different cache configurations, etc. Persons desiring a faster processor would have to purchase a new system or switch out the existing processor of the system for an entirely new processor. Applicants' invention addresses this need for greater processing capability in an existing system by implementing what is now referred to as "hot-pluggable" heterogenous processor functionality.

As noted above, Examiner does recognize the inherent differences in the homogenous environment and the heterogenous environment described by the references. Examiner thus reaches an incorrect conclusion on page 4 of the Office Action that "one skilled in the art... would recognize the benefit it (sic) adding additional processors, from different families." Absent the teachings of Applicants' invention, one skilled in the art would not reach such a conclusion.

Even in one would be inclined to combine the references, the combination still does not suggest the novel features provided by Applicants' claimed invention. For example, Examiner states that *McCrory* has not explicitly taught "higher number of cache levels, larger cache sizes, improved a (sic) cache hierarchy, cache intervention, and larger number of on-chip processors." With the present amendments, Applicants' claims now recite additional functional features

required for implementing cache operations with different cache sizes and cache line widths. None of these features are taught nor suggested by *McCrory* or the combination. *McCrory* also does not provide any suggestion of addition of a heterogenous processor and thus never contemplates the OS functionality required to support the resulting heterogenous configuration.

Notably, there is also no suggestion of connecting the new heterogenous processors to the system via interrupt pins and/or special buses. The interrupt pins provided by *Jayakumar* serves a very different purpose than the expansion functionality provided by the pins described in Applicants' claimed invention. Applicants' use of the term "pins' are inherently different from *Jayakumar's use*, and Applicants have clearly defined the specific use as one with different functionality than a traditional interrupt pin of a processor.

As stated above, Applicants have amended the claims to provide several additional features within that were described in the specification. None of these features are taught or suggested by either of the references or the combination of references. Given the above reasons, it is clear that the combination of references does not suggest Applicants' claimed invention. One skilled in the art would not find Applicants' invention unpatentable over the combination of references. The above claims are therefore allowable.

## CONCLUSION

Applicants have diligently responded to the Office Action by amending the claims to more completely recite the novel features of the invention, clarify the claims, and overcome claim rejections. Applicants have also explained why the amended claims are not taught nor suggested by the references or combination thereof. Since the amendments overcome the §102 and § 103 rejections, Applicants, respectfully request issuance of a Notice of Allowance for all claims now pending.

Applicants also request the Examiner contact the undersigned attorney of record at 512.343.6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,

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**Expires: June 26, 2004**

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Director of Enrollment and Discipline